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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,353	01/28/2004	Jim Paikattu	200314435-1	3291

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EXAMINER	
HOLTON, STEVEN E	
ART UNIT	**PAPER NUMBER**
2629	

NOTIFICATION DATE	DELIVERY MODE
07/20/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/766,353	PAIKATTU ET AL.	
	Examiner	Art Unit	
	Steven E. Holton	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23 and 35-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23,35,36 and 38* is/are rejected.

7)☒ Claim(s) *37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is made in response to applicant's amendment filed on 3/14/2008. Claims 1-23 and 35-38 are currently pending in the application. An action follows below:

Response to Arguments

2. Applicant's arguments with respect to claims 1-23 and 35-38 have been considered but are moot in view of the new ground(s) of rejection based on newly found prior art.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-23, 35, 36, and 38 are rejected under 35 U.S.C. 102(b) as being anticipated by Yoshida et al. (USPN: 6012980), hereinafter Yoshida.

Regarding claim 36, Yoshida discloses an input device including, "a transparent substrate (Fig. 8, element 5); and an array of pixels (Fig. 8, elements P11 to PNM) in physical communication with the substrate, each pixel circuit comprising at least one optical sensor (Fig. 8, element Pc) having a row and column output and (Fig. 8 inset image "example of phototransistor"; row output and column output), and wherein the

row and column output share a common output node of the optical sensor (Fig. 8, inset image; the row and column outputs share a common node with the phototransistor; col. 12, line 30 – col. 14, line 51 describe the embodiment of the invention)."

Regarding claims 22, Yoshida discloses an input device including, "a transparent substrate (Fig. 8, element 5); an array of optical sensors disposed on the substrate (Fig. 8, elements P11 to PNM), the optical sensor array comprising: at least a first optical sensor defining at least one row element (Fig. 8 inset image "example of phototransistor", element Pc, the phototransistor) and at least one column element (Fig. 8 inset image, element Pc, the phototransistor), wherein the row and column element share a common output node of the optical sensor (Fig. 8 inset image; the Row Output and Column Output are connected to the same node of the phototransistor element Pc); an array of conductive trances disposed on the substrate (Fig. 8, the wiring shown as the grid lines connect to the photosensors to transmit electric signals), the conductive trace array comprising: at least a first conductive trace defining a row signal pathway (Fig. 8, the horizontal running traces are row signal lines) and at least a second conductive trance defining a column signal pathway (Fig. 8, the vertical running traces are column signal lines); and wherein the array of optical sensors generate signals on the array of conductive traces upon excitation of electromagnetic radiation (col. 12, line 30 - col. 14, line 51; the phototransistors turn on upon excitation, which outputs signals on the row and column traces to indicate the location of the excitation point of the array).

Regarding claim 23, the Examine notes that the claim contains similar limitations to claim 22, but replaces conductive traces with "signal means". The Examiner reads the array traces of Yoshida as providing row and column signal means on the substrate for transmitting signals. All other limitations of claim 23 are rejected using the similar arguments from claim 22.

Regarding claim 17, Yoshida discloses a computer system including "a computer (Fig. 7, element 1b); and a display comprising: a screen for displaying images (Fig. 7, element 4); and an input device comprising: a transparent substrate (Fig. 8, element 5); an array of optical sensors disposed on the substrate (Fig. 8 elements P11 to PNM are individual optical sensor sections as shown in the inset image “example of phototransistor”), the optical sensor array comprising: a plurality of pixels arranged in rows and columns (Fig. 8, elements P11 to PNM), each pixel comprising at least a first optical sensor defining at least one row element (Fig. 8 inset image "example of phototransistor", element Pc) and at least a second optical sensor defining at least one column element (Fig. 8 inset image "example of phototransistor", element Pc); an array of conductive trances disposed on the substrate, the conductive trace array comprising: at least a first conductive trace defining a row signal pathway (Fig. 8, the horizontal running traces are row signal lines) and at least a second conductive trace defining a column signal pathway (Fig. 8, the vertical running traces are column signal lines); and wherein the array of optical sensors generate signals on the array of the conductive traces upon excitation by electromagnetic radiation (col. 12, line 30 - col. 14, line 51; the

phototransistors turn on upon excitation, which outputs signals on the row and column traces to indicate the location of the excitation point of the array)."

The Examiner notes that the requirements of a first and second optical sensors in each pixel does not require that the optical sensors be distinct and different from each other. Therefore, a single optical sensor could be used to define both a row and column element and output row and column signals along the traces used to transmit signals. Therefore, Yoshida discloses an array of pixels having a first and second optical sensors defining row and column elements where the first and second optical sensors are the same optical sensor.

Regarding claims 18-21, the first optical sensor has an output for outputting a row signal comprising a first and second state (Fig. 8 inset image "Example of phototransistor", element Row Output). The row output will either be a voltage or ground depending if the transistor has been activated by electromagnetic excitation from the light gun (col. 12, line 65 - col. 14, line 30). Similarly, the column output node for the optical sensor will output the same first or second state as the row signal node to indicate which optical sensor has been activated.

Regarding claim 11, the Examiner notes that this claim contains a subset of the limitations found in claim 17. Therefore, the arguments used for the limitations in claim 17 may be applied to the limitations in claim 11.

Regarding claims 12-15, the first optical sensor has an output for outputting a row signal comprising a first and second state (Fig. 8 inset image "Example of phototransistor", element Row Output). The row output will either be a voltage or

ground depending if the transistor has been activated by electromagnetic excitation from the light gun (col. 12, line 65 - col. 14, line 30). Similarly, the column output node for the optical sensor will output the same first or second state as the row signal node to indicate which optical sensor has been activated.

Regarding claim 16, Yoshida discloses the system having row and column outputs (Fig. 8, elements Dv and Dh).

Regarding claim 1, the Examiner notes that this claim has the limitations of the input device found in claim 17. Therefore, the arguments applied to those limitations in claim 17 can be used to reject the limitations in claim 1.

Regarding claims 2-4, the optical sensor of Yoshida (Fig. 8 inset image "example of phototransistor", element Pc) outputs both a row signal and a column signal and acts as both the first and second optical sensors of the pixel.

Regarding claims 8-10, the first optical sensor has an output for outputting a row signal comprising a first and second state (Fig. 8 inset image "Example of phototransistor", element Row Output). The row output will either be a voltage or ground depending if the transistor has been activated by electromagnetic excitation from the light gun (col. 12, line 65 - col. 14, line 30). Similarly, the column output node for the optical sensor will output the same first or second state as the row signal node to indicate which optical sensor has been activated.

Regarding claim 35, the Examiner notes that the limitations of this claim are closely related to the limitations of claim 1. The "conductive means" of claim 35 are

analogous to the "array of conductive traces" of claim 1. The arguments of claim 1 can be further used to rejected claim 35.

Regarding claim 38, Yoshida discloses an input device including a transparent substrate (Fig. 8, element 5) and an array of pixel circuits (Fig. 8, elements P11 to PNM) with each pixel containing a first and second optical sensor (Fig. 8 inset image "example of phototransistor"; element Pc acts as both the first and second optical sensor) and the row output node for a pixel is connected to all other pixel circuits in the row (Fig. 8, the output traces for each row so that row outputs from all pixels in the row are connected) and the column output node for a pixel is connected to all other pixel circuits in the column (Fig. 8, the output traces for each column so that column outputs from all pixels in the column are connected).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5-7 rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshida.

Regarding claim 5, Yoshida discloses that the light sensor panel is transparent (col. 14, line 37-39). However, Yoshida does not expressly disclose the light sensor panel comprises glass.

The Examiner takes Official Notice that the use of glass for making transparent substrates is well known in the art of transparent panels. At the time of invention it would have been obvious to one of ordinary skill in the art that the transparent panel disclosed by Yoshida could be modified to contain a glass as part of the panel composition. This would have been obvious based on the knowledge that glass is transparent and can be used to form panels for holding electronics. Thus, it would have been obvious to use a transparent panel comprising glass or other suitable optically transparent materials.

Regarding claims 6 and 7, Yoshida does not expressly disclose using visible light or infrared light as the form of electromagnetic radiation used to excite the optical sensors. Yoshida does disclose the requirement that the optical sensors are adjusted to respond to the frequency of light emitted from the pointing device (col. 13, lines 47-52).

The Examiner takes Official Notice that optical sensors capable of sensing visible or infrared light are well known in the art of optical sensors. At the time of invention it would have been a matter of design choice for one of ordinary skill in the art to use either visible light or infrared light as the frequency light emitted from the pointing device for excitation of the sensor array. The use of a particular frequency of light would be selected based on cost of optical sensors for a particular frequency of light, the expected environment to use the sensor system in, or even the durability of the different types of optical sensors available for different types of light. Thus, it would have been

obvious to design an input device having optical sensors capable of being excited by visible light or infrared light.

Allowable Subject Matter

5. Claim 37 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The present invention is directed to a input sensor having optical sensors in an array. Claim 37 identifies the uniquely distinct features "the row and column common output node of each pixel circuit is isolated from other pixel circuit row and column common output nodes". The closest prior art, Yoshida discloses row and column output nodes of pixels are commonly connected before transmission to a processing unit, and fails to anticipate or render the above underlined limitations obvious.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven E. Holton whose telephone number is (571)272-7903. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Bipin Shalwala/
Supervisory Patent Examiner, Art Unit 2629

/Steven E Holton/
Examiner, Art Unit 2629
July 14, 2009